Oussama Belhenniche

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EDUCATION:

Bachelor of Engineering (Electrical) **2012-2016**
Ryerson University, Toronto, ON

Coursework:

- Engineering Algorithms and Data Structures
- Software systems
- Object-oriented programming
- Design of Embedded Systems
- ARM Processor Architecture
- HPS/FPGA systems
- Digital Image Processing
- Machine Learning Algorithms (Neural Networks, Linear Regression, Logistic Regression, K-means, Dimensionality Reduction)
- Intelligent Systems
- Digital Systems
- Control Systems
- Microprocessor Systems
- CMOS Mixed-Mode Circuits and Systems
- System Testing and Design-for-Testability
- Systems-on-Chip Design
- Radio-Frequency Circuits and Systems
- Signals and Systems
- Communication theory
- Digital Signal Processing

Skills and Qualifications:

- **Programming Languages**: C/C++, Java, Python, Matlab, Assembly
- **Operating systems**: Unix, Windows, MacOSX
- **IDEs:** Eclipse, Netbeans, CodeWarrior, Code Composer Studio, uVision
- **Simulation Tools:** ModelSim, Cadence, MultiSim, SIMULINK, Pspice, Quartus
- **Hardwar Description languages:** Verilog HDL
- **Publishing Software:** MS Office, Latex
- **Web development:** HTML/CSS, Bootstrap
- **Electronic test equipment:** Power supplies, Oscilloscopes, Multimeters, Function Generators, Spectrum Analyzers
- **Languages:** English, Arabic, French

PROJECTS:

Hardware:

Designed a three-stage differential IC amplifier:

- Design of three-stage cascode differential IC amplifier using IBM's 130nm technology.
- Implementing common-mode feedback.
- Gain of 54dB was achieved, with output resistance of 108 ohms.

Designed a voltage-controlled function generator:

- Design of a linear VCFG using 741 Op-amps.
- Designed for Triangular/ square output.
- Both frequency and amplitude are user-scalable.

Designed an analog low pass filter:

- Design of Butterworth filter using 741 Op-amp.
- Filter's Bandwidth was designed to be 2kHz.

Designed a 1st order delta-sigma AD converter:

- Cadence was used as a development environment.
- IBM's 130nm technology was used.

Implemented MD5 Decryption on HPS/FPGA system:

- SoC designed for MD5 Decryption using DE1-SoC Development board from Altera.
- The MD5 core consisted of 32 engines that compute hashes.
- Avalon MM slaves were created for data and control to interface the IP core to the HPS/FPGA system.
- HPS application coded in C was created using ARM Eclipse that run on a Yocto Linux OS for. HPS application used for feeding the MD5 engines the message either serially or concurrently.

Software:

Implementing sorting algorithms using C programming language.

- Merge sort
- Insertion sort.
- Heap Sort.

Implementing Finite Sate Machine using C programming language.

- FSM was implemented with 4 states.
- States transition's conditions can be changed upon request.
- Unreachable state can be identified and deleted upon request.

Implementing a Media center on the Keil MCB1700 embedded system.

- Designed and implemented a game on the ARM Cortex M3 processor-based device
- User input was taken from the joystick on the board, and the graphical interface was implemented on the LCD
- Photo gallery, and audio streaming were also implemented as part of the media center

Capstone project:

Video-Guidance System For Automated Quadcopter Drone Flight Control:

- Raspberry pi Microcontroller was used with onboard camera on a static platform to detect the Drone position and its direction.
- The drone was equipped with a "Drone attachment" that hosts 4 flashing LEDs in an L-shape arrangement.
- The camera was set to take a picture when the LEDs are ON and another when the LEDs are OFF, and then perform image subtraction to eliminate static noise (Sun)
- Algorithms used include: K-means, Collinearity search, and image processing algorithms.
- Control signals sent from the Microcontroller will try to center the drone on the picture and in a specific direction using the L-shaped LEDs.
- Once the drone is in the middle of the image, the Microcontroller will send the landing signal to the drone.